

Fully Integrated Received Signal Strength Indicator for a Transimpedance Amplifier

Field of the Invention

[001] The invention relates to the field of received signal strength indicator circuits and more specifically in the field of received signal strength indicator circuits integrated with transimpedance amplifier circuits.

Background of the Invention

[002] The ever increasing demands for high capacity communications systems has resulted in a wide spread deployment of optical fiber networks across the world. A fundamental component used in such systems receives pulses of light and converts these into electrical signals. The pulses of light in such systems comprise a bit stream of information. This fundamental component employed in fiber optic networks is commonly known as an optical receiver module. Within the optical receiver, a photodetector is typically employed to receive light pulses and an amplifying circuit is employed for amplifying photocurrent generated within the photodetector.

[003] Transimpedance amplifiers (TIAs) are typically used within optical receiver modules to amplify and transform weak photocurrents received from the photodetector, typically a photodiode or a PIN diode. The TIA amplifies and transforms the photocurrent into an output voltage that is further provided to other stages of the optical receiver module. Since TIAs are used to deal with both strong and weak photocurrents, noise in the resultant amplified and transformed voltage signal is typically a problem. Indeed, for those skilled in the art of the design of TIAs, it is well understood and appreciated that the noise introduced by the TIA, in many circumstances, limits the ability of the optical receiver module to faithfully reconstruct the intended stream of information. Furthermore, a relationship between the rate at which errors are produced by the receiver – often called the Bit Error Rate (BER), and the noise generated by the TIA can be shown. Thus, the optical receiver module needs to have low noise amplification performed on weak photocurrents in order to facilitate optical transmission of

information. This is especially true in circumstances where the distance that the optical signal must travel is long and results in weak optical pulses at the receiver. It is known to those skilled in the art that long transmission distances – the distance between a transmitter and a receiver - serves to attenuate the initial transmitted optical signal strength and places a greater burden upon the receiver module to avoid errors. Furthermore, it is also known that cost of an optical communication system is reduced if a signal is transmitted along a longer length of optical fiber or, in the alternative, if less optical power is transmitted. Thus, providing low noise amplification for the TIA is important in order to reduce bit error rate (BER) of the received and amplified signal.

[004] In optical receiver systems, the photodiode and TIA are typically co-packaged within a single module. After co-packaging, once the position of the photodiode is fixed in relation to a housing of the received module, an optical fiber is aligned to the photodiode in order to provide the pulses of light propagating in the optical fiber to the photodiode. Proper optical alignment of the optical fiber to the photodiode is critical in order to minimize optical coupling loss therebetween and in order to utilize a full dynamic range of the photodiode and TIA coupled therewith. In performing of optical alignment of the optical fiber to the photodiode, light is typically propagated through the optical fiber and a signal indicative of the quality of the alignment is provided from the TIA in order to obtain optimal positional alignment of the optical fiber.

[005] In performing of this optical alignment, the light incident upon the photodiode always has a mean DC component and this DC component represents the mean signal strength of the optical signal as received by the photodetector and amplified by the TIA. Typically, the signal indicative of the quality of the alignment is in the form of a Received Signal Strength Indicator (RSSI) signal provided from an RSSI output port on the TIA. A magnitude of the RSSI signal represents the mean optical signal strength, which is used to align the photodiode detector to the optical fiber within the receiver module to achieve maximum responsivity during the manufacturing process or to provide an analog indication of the mean optical power incident upon the receiver for further processing during operation. This RSSI represents the mean DC current, or ratio of current, flowing through the photodiode detector into an input port of the TIA.

[006] Often circuits that provide the RSSI signal are implemented externally from the TIA and are disposed in such a manner so as to monitor the DC current flowing at the cathode of a photodiode detector. This method unfortunately reduces the reverse bias voltage if a PIN diode detector is used. For single ended power supply operation this proves to be a problem, especially when 3.3V single ended power supply voltages are used.

[007] An alternative approach to providing of the RSSI signal is to rectify the TIA output signal from the TIA and provide a Root Mean Squared (RMS) component of this signal that is representative of the RSSI. This, however, is not a true RSSI, since most TIAs exhibit automatic gain control (AGC) or signal limiting within the full optical dynamic range of the TIA and thus the RSSI is not a true representation of the DC current flowing through the photodetector and into the TIA.

[008] A need therefore exists to provide a RSSI circuit that is representative of the coupling of the optical fiber to the photodiode without a reduction in the reverse bias voltage provided to the photodiode. It is therefore an object of the invention to provide an integrated RSSI circuit integrated with the TIA that does not reduce the reverse bias voltage when used with a photodetector in the form of a PIN photodiode. Furthermore, it is an object of the invention to provide an integrated RSSI circuit that can operate from the same voltage supply used by TIA. Furthermore, it is an object of the invention to provide an integrated RSSI circuit integrated with the TIA that does not introduce a sensitivity penalty due to a DC voltage offset between the active TIA and the reference TIA.

Summary of the Invention

[009] In accordance with the invention there is provided a circuit for coupling to a photodetector for providing a received signal strength indicator (RSSI) signal comprising: a transimpedance amplifier (TIA) stage coupled to the photodetector for receiving current flowing therethrough and for providing a TIA output signal; a filter circuit having an input port for receiving the TIA output signal and for filtering the TIA output signal to

provide a first voltage signal; a dummy TIA stage having a dummy TIA output port for providing a second DC voltage signal; a high gain integrator circuit having a negative input port for receiving the second DC voltage signal, having a positive input port for receiving the first voltage signal and having an output port for providing a high gain integrator output signal therefrom; a transconductance amplifier (TCA) circuit having a negative input port for receiving the second DC voltage signal, having a positive input port for receiving the first voltage signal, and having an output port for providing a first current therefrom; and a second current mirror having an input port for receiving the first current and a second current and for providing the RSSI signal from an output port thereof, the RSSI signal dependent upon the first and second currents.

[0010] In accordance with the invention there is provided a method of providing a RSSI signal from a circuit coupled to a photodiode comprising the steps of: propagating a photodiode current through the photodiode; providing a transimpedance amplifier (TIA) circuit for providing of a TIA output signal in dependence upon receiving of the photodiode current from the photodiode; adjusting a first bias voltage; providing a first current in dependence upon the photodiode current and the first bias voltage; providing a second current in dependence upon the photodiode current and the first bias voltage; and, summing the first and second currents to provide an added current, where the RSSI signal is dependent thereon.

Brief Description of the Drawings

[0011] Exemplary embodiments of the invention will now be described in conjunction with the following drawings, in which:

[0012] FIG. 1a illustrates common, prior art, circuit used for providing a RSSI signal from a circuit that operates with a single positive supply voltage;

[0013] FIG. 1b illustrates common, prior art, circuit used for providing a RSSI signal from a circuit that operates using two positive supply voltages;

[0014] FIG. 2 illustrates an alternative circuit for providing a RSSI signal by implementing a DC restoration control loop;

[0015] FIG. 3 illustrates a circuit architecture used for generating a RSSI signal in accordance with an embodiment of the invention; and,

[0016] FIG. 4 graphically illustrates the RSSI output signal, in the form of RSSI output current, with respect to a mean photodiode output current.

Detailed Description the Invention

[0017] FIG. 1a illustrates a common, prior art, circuit used for providing a RSSI signal. In this circuit, a current mirror 113, formed from MOSFETS M1 151 and M2 152 is coupled in series with a cathode terminal of a photodiode 107. An output port 113b of the current mirror 113 is used for providing the RSSI signal therefrom. A P-channel MOSFET M1 151 is disposed in a diode configuration, with a gate terminal of MOSFET M1 151 connected to a gate terminal of MOSFET M2 152 to provide a gate-source potential having a sufficient magnitude for enabling of the P channel MOSFET M2 152 to act as a first current source. If the geometry of MOSFETs M1 151 and M2 152 are the same, the current at the drain terminal of MOSFET M1 151 is equal to the drain current of MOSFET M2 152. This drain current, emitted from the current mirror output port 113b, provides the RSSI signal having a one to one relationship with a DC photodiode current propagating through the photodiode 107. A transimpedance amplifier (TIA) circuit 103 is provided with a TIA input port 103a connected to the photodiode 107 anode terminal and a TIA output port 103b for providing an output signal. A first feedback resistor 161 is disposed between the TIA input port 103a and the TIA output port 103b establishing a gain of the TIA 103. A first supply voltage input port 100a is provided for receiving a positive supply voltage (V_{pos}) and a second supply voltage input port 100b is provided for receiving a negative supply voltage (V_{neg}) for energizing of the current mirror 113 and the TIA 103. The negative supply voltage (V_{neg}) is for receiving a ground voltage.

[0018] The supply voltage, V_{pos} , provided to the first voltage supply input port 100a, is 3.3V and the potential drop across the source-drain terminals of MOSFET M1 151 is marginally higher than the threshold voltage of MOSFET M2 152. Of course, this is dependent upon geometry of the MOSFETs and the drain current of MOSFET M1 151. This potential drop across the source-drain terminals of MOSFET M1 151 unfortunately lowers the reverse bias voltage available to the photodiode 107. Lowering of the reverse bias voltage unfortunately decreases the dynamic range operation of the photodiode 107 especially at long wavelengths (1300-1500nm) and at high optical data rates (10Gbit/s). Typically for these wavelengths and optical data rates, photodiode operation with a 2V reverse bias voltage is preferred.

[0019] Of course, if the TIA is optionally designed to operate at 5V and to provide an input bias voltage that is as low as possible, approximately one V_{be} , in which case the addition of the current mirror 113 formed by MOSFETS M1 151 and M2 152 would not substantially reduce the reverse bias voltage provided to the photodiode 107.

[0020] An alternative circuit used for providing additional reverse bias voltage to the photodiode 107 is shown in prior art FIG. 1b, which is a variation of the circuit shown in FIG. 1a. In this variation, the TIA 103 operates using a potential received from the first voltage supply input port 100b, and operates using a $V_{pos2}=3.3V$ supply voltage. A third supply voltage input port 100c is provided for providing a higher potential than V_{pos2} , where $V_{pos1}=5V$. V_{pos1} is provided to the current mirror 113a, formed from MOSFETs M1 151a and M2 152a, for reverse biasing of the photodiode 107 using this separate supply voltage, V_{pos1} . Similar to that of FIG. 1a, the current mirror 113a provides the RSSI signal. By using two positive supply voltages, V_{pos2} and V_{pos1} , the reverse bias voltage of the photodiode 107, in the form of a PIN diode, is advantageously not lowered, as is the case in FIG. 1a. However this is accomplished at the expense of utilizing two positive supply voltages. In addition, if the photodiode is in the form of an avalanche photodiode detector (APD), the cathode is coupled to a separate supply positive voltage supply of approximately 55-60V, in which case the circuit shown in FIG. 1a is not useable. In using the circuit shown in FIG. 1b, external P-MOSFET devices are used when this circuit is used in conjunction with an APD.

[0021] FIG. 2 illustrates a circuit for providing a RSSI signal by implementing a DC restoration control loop. The output port 203b of a TIA stage 203 is coupled to a negative input port 210b of an operational amplifier (OpAmp) 210, via a resistor R1 221. The OpAmp 210 is configured as an integrator, with a capacitor C1 231 connected between an OpAmp output port 210c and an OpAmp negative input port 210b. A first feedback resistor 261 is coupled from the TIA output port 203b to the TIA input port 203a.

[0022] A dummy TIA stage 204 is used to provide a same DC output voltage as a DC output voltage of the TIA 203, via a resistor R2 222, to a positive input port of the OpAmp 210. The resistors R1 221 and R2 222 are designed to be equal in value to minimize DC voltage offsets between the positive and negative input signals received on the input ports 210a and 210b of the OpAmp 210. The output port of the integrator circuit 210c, which is the OpAmp output port 210c, is coupled to a voltage controlled current source formed by transistor Q2 242 and resistor R3 223. The collector terminal of transistor Q2 242 is connected to the TIA input port 203a and to the anode of the photodiode 207. Since the TIA 203 and dummy TIA 204 stages are identical, the DC potential difference between the input ports of the integrator circuit, which are the input ports of the OpAmp 210, are zero, and thus no current flows into the collector terminal of transistor Q2 242.

[0023] Upon an application of an unmodulated optical signal to the photodiode, the unmodulated optical signal causes a shift in the DC level of a current flowing through the photodiode and into the TIA input port. This results in an input signal provided to the negative input port 210b of the integrator circuit (210 and 231) to be less than the input signal provided to the positive input port 210a, resulting in the integrator circuit (210 and 231) causing a current to be provided at the collector terminal of transistor Q2 242 to be equal to the DC current flowing through the photodiode 207 and into the TIA input port 203a.

[0024] The TIA output signal is thus 'clamped' and has a DC output signal level that is the same as that of the dummy TIA stage output signal DC level. By providing a current mirror formed from transistor Q1 241 and resistor R4 224, an exact replica, or portion, of

the current at the collector terminal of transistor Q2 242 appears at the collector terminal of transistor Q1 241. This collector current is applied to a second current mirror 213 formed from P channel MOSFETs M1 251 and M2 252, where the drain terminal of MOSFET M2 252 serves as an RSSI signal output port for providing of the RSSI signal.

[0025] The circuit for generating of the RSSI signal shown in FIG. 2 operates in response to a 3.3V supply without reducing the photodiode's reverse bias voltage, and in addition, also operates if the photodiode is an APD, which requires an external bias voltage of 55-60V. However, in practice, DC voltage mismatches between the TIA output signal and the dummy TIA output signal cause a DC voltage offset to be observed between the output ports of the TIA and the dummy TIA.

[0026] If TIA output signal DC voltage is marginally more negative than the DC output voltage at the dummy TIA, this causes the collector current of transistor Q2 242 to flow into the TIA input port 203a and to clamp the DC voltage output signal of the TIA stage 203. This clamping results in the DC output signal level of the dummy TIA stage 204 to be equal to the DC voltage output of the TIA stage 203, thus causing a noise penalty due to additional shot noise from the collector current of transistor Q2 242.

[0027] FIG. 3 illustrates a circuit architecture used for generating a RSSI signal in accordance with an embodiment of the invention. The circuit shown in FIG. 3 is comprised of four main circuit blocks. These circuit blocks are a TIA stage 303, a Dummy TIA stage 304, a High Gain Integrator (HGI) circuit 305 and a Transconductance Amplifier (TCA) circuit 306. A first supply voltage input port 300a is provided for receiving a Vpos voltage, where each of the circuit blocks are connected to the first supply voltage input port 300a for receiving of Vpos, and a second supply voltage input port 300b is provided for receiving of a preferably ground voltage, where each of the circuit blocks are connected to these supply voltage input ports for energizing of circuitry within the circuit blocks. A photodiode 307 is coupled with its anode terminal to a TIA input port 303a, while its cathode terminal is coupled to the first supply voltage input port 300a. A first feedback resistor 361 is disposed between the TIA input port 303a and a TIA output port 303b. The TIA output port 303b is coupled to a filter input port 308a of a

filter circuit 308 in the form of a low pass filter circuit formed by resistor R1 321 and capacitor C1 331. Capacitor C1 331 functions as a filter capacitor within the low pass filter circuit. A filter circuit output port 308b is coupled to a positive input port 309a of a first differential amplifier 309, disposed within the HGI 305, via a second HGI input port 305a, for providing a filtered output signal, in the form of first voltage signal (V1) thereto. A second feedback resistor 362 is disposed between a dummy TIA stage input port 304a and a dummy TIA stage output port 304b. A DC output signal is provided from the dummy TIA stage 304 from the dummy TIA stage output port 304b to a negative input port 309b of the differential amplifier 309, via a first HGI input port 305b and a resistor R2 322, for providing a second DC voltage signal (V2) to the first differential amplifier 309. This second DC voltage signal (V2) is provided under a condition when the photodiode 307 receives approximately no light. The resistors R1 321 and R2 322 are designed to have equal resistances in order to minimize DC voltage offsets occurring due to the positive and negative input bias currents of the first differential amplifier 309. A first differential amplifier output signal is provided from the first differential amplifier 309 via a resistor R3 323 to a negative input port of a first Op-Amp 310b. The first differential amplifier 309 provides an output signal that is a difference voltage between V1, the input signal on port 305b, and V2, the input signal on port 305a. This output signal is adjustable, by adjusting a first bias signal, for providing unity gain.

[0028] This difference voltage is applied to a negative input port 310b of a first operational amplifier (first OpAmp) 310 via a resistor R3 323 and capacitor C4 334. The first OpAmp, third resistor 323 and fourth capacitor 334 are disposed in an integrator configuration. An output port 310c of the first OpAmp 310 is coupled to the High Gain Integrator output port 305c for providing a HGI output signal therefrom.

[0029] The HGI output port 305c is connected to a voltage controlled second current source formed by transistor Q2 342 in series with a resistor R8 328 disposed between the emitter terminal and the second supply voltage input port 300b. The collector terminal of transistor Q2 342 is also coupled to the anode terminal of the photodiode 307. This connection to the anode terminal of the photodiode 307, and thus to the input port 302a of the TIA 203, provides a DC feedback path in this closed loop configuration.

[0030] A positive input port 310a of the first Op-Amp 310 is for receiving of the first bias signal. A voltage of this first bias signal is used to predetermine a reference voltage (V_{ref}) for the first Op-Amp 310 for resulting in a light intensity incident upon the photodiode 307 to be sufficiently above a noise floor before a collector current of transistor Q2 342 is used to 'clamp' a DC portion of the TIA output signal provided from the TIA output port 303b. The base terminal of transistor Q2 342 is additionally connected to a first current mirror circuit formed by transistor Q1 341 and resistor R9 329 disposed between an emitter terminal of transistor Q1 341 and the second supply voltage input port 300b. The first current mirror, generating a current I_2 is of such a configuration that the collector current of transistor Q1 341 is preferably equal to the collector current of transistor Q2 342.

[0031] The potentials V_1 and V_2 are also applied to first and second TCA input ports 306a and 306b. A second difference amplifier 311 is disposed within the TCA 306 for receiving the potentials V_1 and V_2 using a positive input port 311a and a negative input port 311b, respectively. Differential output signals from the second difference amplifier 311 are applied to a differential integrator circuit formed by resistors R4 324, R5 325, R6 326, R7 327 and capacitors C2 332 and C3 333, and a second OpAmp 312, as shown in FIG. 3. Resistors R4 324 and R6 326 are disposed between first and second output ports of the second differential amplifier 311 and negative and positive input ports, 312b and 312a, of the second OpAmp 312. An output port 312c of the second OpAmp 312 is connected to a base terminal of transistor Q3 343 for providing of a differential integrator output signal, in the form of a differential integrator output current, thereto.

[0032] A third feedback resistor 363 is disposed between the emitter terminal of the third transistor Q3 343 and the second supply voltage input port 300b. Preferably the resistance of the third feedback resistor 363 is selected to be approximately identical to that of the first feedback resistor 361 disposed within the TIA stage 303 and the second feedback resistor 362 disposed within the dummy TIA stage 304.

[0033] The emitter terminal of transistor Q3 343 is also coupled in series with resistor R7 327 and capacitor C2 332, disposed in parallel and coupled in series with the

negative input port 312b of the second OpAmp 312. The differential integrator circuit output port 306c is formed from the collector terminal of transistor Q3 343 for providing a first current therefrom.

[0034] If a second gain of the second differential amplifier 311 is set to unity, and $R4=R7=R$ and $C2=C3=C$, a transconductance gain of the TCA 306 is expressed in Equation (1):

$$\text{a. } I_1 = \frac{1}{R_{F1}} \times \frac{V_1 - V_2}{1 + S \cdot C \cdot R} \quad (1)$$

[0035] Therefore the TCA output signal provides an output current I_1 dependent upon the difference voltage ($V_1 - V_2$) of the TIA output signal and the dummy TIA output signal, divided by an effective transimpedance gain, which is dependent upon the first feedback resistor 361 disposed with the TIA stage 303. S is the Laplace Operator showing the integration action determined by the time constant set by $C \cdot R$.

[0036] A pole formed from resistor $R1$ 321 and capacitor $C1$ 331 of the filter circuit 308 performs filtering of a portion of noise in the TIA output signal. The collector terminal of transistor Q3 343 is connected to the collector terminal of transistor Q1 341, this results in an addition of currents I_1 and I_2 , to form an added current. A second current mirror 313 is formed from P channel MOSFETs M1 351 and M2 352. Source terminals of MOSFETs M1 351 and M2 352 are connected to the first supply voltage input port 300a. A second current mirror input port 313a is connected to the collector terminal of transistor Q1 341 of the first current mirror and to the collector terminal of transistor Q3 343 of the third current source. The second current mirror input port 313a receives the added current, where within the second current mirror 313 this added current is provided to gate terminals of MOSFETs M1 351 and M2 352, as well as to the drain terminal of MOSFET M1 351. MOSFET M1 351 is disposed in a diode configuration. The drain terminal of MOSFET M2 352 forms the second current mirror output port 313b for providing of the RSSI signal therefrom. Typically, the drain current of MOSFET M1

351 is set to be equal to the drain current of MOSFET M2 352, or set to some multiple of the drain current of MOSFET M2 352.

[0037] FIG. 4 graphically illustrates the RSSI output signal, in the form of RSSI output current, with respect to a mean photodiode output current. The second current (I_2) 402 represents a DC restoration loop current for the collector terminal of transistor Q2 342. This second current (I_2) 402 on its own does not represent the mean current flowing through the photodiode 307. The first bias signal (V_{ref}) applied to the positive input port 310a of the first OpAmp 310 is used to provide the reference voltage (V_{ref}), where this first bias signal (V_{ref}) ensures that substantially no current flows from the TIA input port 303a until a threshold input current 404 provided to the TIA input port 303a is reached. FIG. 4 illustrates an exemplary threshold current 404 of 200uA. Above this threshold current 404, I_2 402 increases with increasing DC photodiode current. This ensures that the DC output voltage of the TIA output signal remains clamped. The current I_1 401 operates between zero photodiode current, the sensitivity limit of the photodiode, up to the threshold current 404, as determined by first bias signal, since the current I_2 402 is determined by the potential difference of $V_1 - V_2$. Above the threshold current 404, I_1 401 remains constant since the DC component of the TIA output signal is clamped, such that $V_1 - V_2 = 0$. By adding the collector currents of transistors Q3 343 and Q1 341, the total current, $I_1 + I_2$ represents the total mean current flowing through the photodiode 307 and into the TIA input port 303a.

[0038] Advantageously, when the circuit of FIG. 3 is utilized, the photodiode cathode is directly connected to the first supply voltage input port 300a and thus a maximum reverse bias voltage is provided to the photodiode 307. In addition, the circuit illustrated in FIG. 3 operates from a single ended 3.3V power supply ($V_{pos} = 3.3V$) as opposed to requiring a dual V_{pos} power supply, as that which is utilized with the circuit of FIG. 1b. In addition, the circuit of FIG. 3 advantageously allows for an avalanche photodiode (APD) to be used therewith. When an APD is used, then the APD is advantageously operated from a separate power supply, if required. Thus an APD is useable in place of the photodiode without any hindrance to the fully integrated RSSI circuit, with the circuit still for providing the RSSI signal to the RSSI output port 313b thereof.

[0039] Advantageously, the fully integrated RSSI circuit utilizes a threshold current to ensure that the DC restoration loop does not cause a signal receiver sensitivity penalty due to a mismatch between the DC output voltage of the TIA stage 303 and dummy TIA stage 304. The TCA 306 provides the first current (I_1) from zero photodiode current, the sensitivity limit of the photodiode, up to the threshold current 404 and is advantageously included within the fully integrated RSSI circuit.

[0040] Numerous other embodiments may be envisaged without departing from the spirit or scope of the invention.